Application No.: 09/540,828

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (previously presented) A system interface comprising:

a plurality of first directors;

a plurality of second directors;

a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

a message network, operative independently of the data transfer section, coupled to the plurality of first directors and the plurality of second directors; and

wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the message network to facilitate data transfer between first directors and the second directors with such data passing through the cache memory in the data transfer section.

2. (original) The system interface recited in claim 1 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a controller for transferring the messages between the message network and such one of the first directors.

3. (original) The system interface recited in claim 1 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

4. (original) The system interface recited in claim 2 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second director.

5. (original) The system interface recited in claim 1 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and for controlling the data between the input of such one of the first directors and the cache memory.

6. (original) The system interface recited in claim 1 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors

and for controlling the data between the input of such one of the second directors and the cache memory.

7. (original) The system interface recited in claim 5 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

8. (currently amended) A data storage system for transferring data between a host computer/server and a bank of disk drives through a system interface, such system interface comprising:

a plurality of first directors coupled to host computer/server;

a plurality of second directors coupled to the bank of disk drives;

a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

a message network, operative independently of the data transfer section, coupled to the plurality of first directors and the plurality of second directors; and

wherein the first and second directors control data transfer between the host computer/server and the bank of disk drives in response to messages passing between the first directors and the second directors through the message network to facilitate the data transfer between host computer/server and the bank of disk drives with such data passing through the cache memory in the data transfer section.

9. (original) The system interface recited in claim 8 wherein each one of the first

directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a controller for transferring the messages between the message network and such one of the first directors.

10. (original) The system interface recited in claim 8 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

11. (original) The system interface recited in claim 9 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

12. (original) The system interface recited in claim 8 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and for controlling the data between the input of such one of the first directors and the cache

memory.

13. (original) The system interface recited in claim 8 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

14. (original) The system interface recited in claim 12 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

Cancel Claim 15.

Cancel claim 16.

17. (previously presented) A method of operating a system interface having a plurality of first directors, a plurality of second directors and a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors, such

method comprising:

providing a message network, operative independently of the data transfer section, coupled to the plurality of first directors and the plurality of second directors to control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the message network to facilitate data transfer between first directors and the second directors with such data passing through the cache memory in the data transfer section.

18. (original) The method recited in claim 17 including providing each one of the first directors is provided with:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a controller for transferring the messages between the message network and such one of the first directors.

19. (original) The method recited in claim 17 including providing each one of the second directors with:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

20. (original) The method recited in claim 18 including providing each one of the second directors with:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

21. (original) The method recited in claim 17 including providing each one of the first directors with:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and for controlling the data between the input of such one of the first directors and the cache memory.

22. (original) The method recited in claim 17 including providing each one of the second directors with:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

23. (original) The method recited in claim 21 including providing each one of the second directors with:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

Application No.: 09/540,828

24. (previously presnted) The system interface recited in claim 1 wherein the message network comprises a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of first and second directors.

25. (previously presented) A system interface comprising:

a plurality of first directors;

a plurality of second directors;

a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

a message network comprising a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of first directors and second directors, such message network being operative independently of the data transfer section; and

wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the message network to facilitate data transfer between first directors and the second directors with such data passing through the cache memory in the data transfer section.

26. (currently amended) A system interface comprising:

a plurality of first directors;

a plurality of second directors;

a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

a message network, operative independently of the data transfer section, coupled to the plurality of first directors and the plurality of second directors; and

wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the

second directors through the message network with such messages by-passing the data transfer section and with such data transfer comprising passing data through the directors to the cache memory in the data transfer section. [[,]]

27. (previously presented) The system interface recited in claim 26 wherein the message network comprises a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of first and second directors.

28. (previously presented) A system interface comprising:

a plurality of first directors;

a plurality of second directors;

a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

a message network coupled to the plurality of first directors and the plurality of second directors; and

wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the message network with such messages by-passing the data transfer section and with such data transfer comprising passing data through the directors to the cache memory in the data transfer section.

29. (previously presented) The system interface recited in claim 28 wherein the message network comprises a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of first and second directors.

30. (previously presented) A system interface comprising:

a plurality of first directors;

a plurality of second directors;

a data transfer section having a cache memory, such cache memory being

coupled to the plurality of first and second directors;

a message network comprising a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of first and second directors; and

wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the message network with such messages by-passing the data transfer section and with such data transfer comprising passing data through the directors to the cache memory in the data transfer section.

31. (previously presented) A system interface comprising:

a plurality of directors

a data transfer section having a cache memory, such cache memory being coupled to the plurality of directors;

a message network, operative independently of the data transfer section, coupled to the plurality of directors; and

wherein the directors control data transfer in response to messages passing between the directors through the message network with such data passing through the cache memory in the data transfer section.

32. (previously presented) The system interface recited in claim 31 wherein each one of the directors includes:

a data pipe coupled between an input of such one of the directors and the cache memory; and

a controller for transferring the messages between the message network and such one of the directors.

33. (previously presented) The system interface recited in claim 31 wherein the message network comprises a switch network having a plurality of ports, each one of the ports being

coupled to a corresponding one of the plurality of directors.

34. (previously presented) The system interface recited in claim 33 wherein each one of the directors includes:

a data pipe coupled between an input of such one of the directors and the cache memory; and

a controller for transferring the messages between the message network and such one of the directors.

35. (previously presented) A data storage system for transferring data between a host computer/server and a bank of disk drives through a system interface, such system interface comprising:

a plurality of first directors coupled to host computer/server;

a plurality of second directors coupled to the bank of disk drives;

a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

a message network, operative independently of the data transfer section, coupled to the plurality of first directors and the plurality of second directors; and

wherein the first and second directors control data transfer between the host computer/server and the bank of disk drives in response to messages passing between at least a pair of the plurality of first and second directors through the message network with such data passing through the cache memory in the data transfer section.

36. (previously presented) The system interface recited in claim 35 wherein each one of the first and second directors includes:

a data pipe coupled between an input of such one of the first and second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the first and second directors.

37. (previously presented) The system interface recited in claim 35 wherein the message network comprises a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of first and second directors.

38. (previously presented) The system interface recited in claim 37 wherein each one of the directors includes:

a data pipe coupled between an input of such one of the directors and the cache memory; and

a controller for transferring the messages between the message network and such one of the directors.

39. (previously presented) A system interface comprising:

a plurality of directors;

a data transfer section having a cache memory, such cache memory being coupled to the plurality of directors;

a message network, operative independently of the data transfer section, coupled to the plurality of directors; and

wherein the directors control data transfer in response to messages passing between the directors through the message network with such data passing through the cache memory in the data transfer section.

40. (previously presented) The system interface recited in claim 38 wherein each one of the directors include:

a data pipe coupled between an input of such one of the directors and the cache memory;

a controller for transferring the messages between the message network and such one of the directors.

Application No.: 09/540,828

41. (previously presented) The system interface recited in claim 40 wherein the message network comprises a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of directors.

42. (previously presented) The system interface recited in claim 41 wherein each one of the directors includes:

a data pipe coupled between an input of such one of the directors and the cache memory; and

a controller for transferring the messages between the message network and such one of the directors.

43. (previously presented) A system interface comprising:

a plurality of directors;

a data transfer section having a cache memory, such cache memory being coupled to the plurality of directors;

a message network comprising a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of directors, such message network being operative independently of the data transfer section; and

wherein the directors control data transfer in response to messages passing between the directors through the message network with such data passing through the cache memory in the data transfer section.

44. (currently amended) A system interface comprising:

a plurality of directors;

a data transfer section having a cache memory, such cache memory being coupled to the plurality of directors;

a message network, operative independently of the data transfer section, coupled to the plurality of directors; and

wherein the directors control data transfer in response to messages passing between the directors through the message network with such messages by-passing the data transfer section and with such data transfer comprising passing data through the directors to the cache memory in the data transfer sections. [[.]]

45. (previously presented) The system interface recited in claim 44 wherein the message network comprises a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of directors.

46. (previously presented) A system interface comprising:

a plurality of directors;

a data transfer section having a cache memory, such cache memory being coupled to the plurality of directors;

a message network coupled to the plurality of directors; and

wherein the first and second directors control data transfer in response to messages passing between the directors through the message network with such messages by-passing the data transfer section and with such data transfer comprising passing data through the directors to the cache memory in the data transfer section.

47. (previously presented) The system interface recited in claim 46 wherein the message network comprises a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of directors.

48. (previously presented) A system interface comprising:

a plurality of directors;

a data transfer section having a cache memory, such cache memory being coupled to the plurality of directors;

a message network comprising a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of

Application No.: 09/540,828

directors; and

wherein the directors control data transfer in response to messages passing between the directors through the message network with such messages by-passing the data transfer section and with such data transfer comprising passing data through the directors to the cache memory in the data transfer section.

Cancel claims 49-56.

57. (currently amended) A system, comprising:

a first director;

a second director;

a cache memory coupled to the first director and the second director;

a message network coupled to the first director and the second director;

wherein the first and second directors control data transfer between first director and the second director with the data in the data transfer passing through the cache memory in response to messages passing between the first director and the second director through the message network; and

wherein the messages passing through the message network by-pass the cache memory. [[.]]

58. (previously presented) A system, comprising:

a first director;

a second director;

a cache memory;

a message network coupled to the first director and the second director;

wherein the first and second directors control data transfer between first director and the second director with data in such data transfer passing through the cache memory in response to messages passing between the first director and the second director through the message network; and

wherein each one of the messages includes a destination field.

59. (previously presented) A data storage system for transferring data between a host computer/server and a bank of disk drives through a system interface, such system interface comprising:

a plurality of first directors coupled to host computer/server;

a plurality of second directors coupled to the bank of disk drives;

a cache memory, such cache memory being coupled to the plurality of first and second directors;

a message network coupled to the plurality of first directors and the plurality of second directors;

wherein the first and second directors control data transfer between the host computer/server and the bank of disk drives with data in such data transfer passing through the cache memory in response to messages passing between the first director and the second director through the message network; and

wherein the messages passing through the message network by-pass the cache memory.

Cancel claim 60.

61. (currently amended) A [[.]] system, comprising:

a plurality of first directors;

a plurality of second directors;

a cache memory;

a message network, coupled to the plurality of first directors and the plurality of second directors;

wherein the cache memory is coupled the plurality of first directors and to the plurality of second directors;

wherein data is transferred between first directors and the second directors

through the cache memory in response to messages passing between the first directors and the second directors through the message network; and

wherein the messages passing through the message network by-pass the cache memory.

62. (previously presented) The system recited in claim 61 wherein the each one of the messages comprises a packet, such packet having a destination field.

Cancel claim 63.

64. (previously presented) A system, comprising:

a first director;

a second director;

a cache memory;

a message network, coupled to the first director and the second director;

wherein where the cache memory is coupled the first director and to the second director;

wherein data is transferred between the first director and the second director through the cache memory in response to messages passing between the first director and the second director through the message network; and

wherein the messages passing through the message network by-pass the cache memory.

65. (previously presented) The system recited in claim 64 wherein the each one of the messages comprises a packet, such packet having a destination field.

Cancel claim 66.

67. (previously presented) A system, comprising:

a plurality of directors, each one having a data port for data and a separate message port for messages;

a cache memory coupled to the data ports of the plurality of directors;

a message network coupled to the message ports of the plurality of directors;

wherein the plurality of directors control data transfer between the directors with said data in such data transfer passing through the cache memory in response to said messages passing between the directors through the message network; and

wherein the messages passing through the message network by-pass the cache memory.

68. (previously presented) The system recited in claim 67 wherein each one of the messages includes a destination field.

69. (previously presented) A system, comprising:

a plurality of directors, each one having message port for messages;

a cache memory coupled to the plurality of directors;

a message network coupled to the message ports of the plurality of directors;

wherein the plurality of directors control data transfer between the directors with said data in such data transfer passing through the cache memory in response to said messages passing between the directors through the message network; and

wherein with messages passing through the message network by-pass the cache memory.

70. (previously presented) The system recited in claim 69 wherein each one of the messages includes a destination field.

71. (previously presented) The system recited in claim 73 wherein each one of the messages includes a destination field.

Application No.: 09/540,828

Cancel claim 72.

73. (previously presented) A system, comprising:

a plurality of directors, each one having message port for messages;

a cache memory in communication with the plurality of directors;

a message network coupled to the message ports of the plurality of directors;

wherein the plurality of directors control data transfer between the directors with said data in such data transfer passing through the cache memory in response to said messages passing between the directors through the message network; and

wherein the messages passing through the message network by-pass the cache memory.

74. (previously presented) The system recited in claim 73 wherein each one of the messages includes a destination field.

Cancel claim 75.

76. (previously presented) A data storage system for transferring data between a host computer/server and a bank of disk drives through a system interface, such system interface comprising:

a plurality of directors coupled to the host computer/server and to the bank of disk drives;

a global memory accessible to the plurality of directors through arbitration;

a message network coupled to the plurality of directors, such directors controlling data transfer between the host computer/server and the bank of disk drives in response to messages passing between the directors through the message network as such data passes through the memory with such messages by-pass the cache memory.

77. (previously presented) The data storage system recited in claim 76 wherein the message

network includes a plurality of ports each one coupled to a corresponding one of the plurality of directors.

78. (previously presented) The data storage system recited in claim 77 wherein the message network is a packet switching network and wherein the messages are packets for passing between the ports through the packet switching network.